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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/816,071	03/30/2004	Xinping He	384938080US	8904

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EXAMINER	
WILSON, ALLAN R	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 11/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/816,071	HE, XINPING	
	Examiner	Art Unit	
	Allan R. Wilson	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *0604*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the transistor in the semiconductor substrate must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2 and 4-6 are rejected under 35 USC § 102(b) as being anticipated by Inoue et al. ("Inoue") U.S. Patent No. 6,211,509.

With regards to claim 1, Inoue illustrates in figures 1A-7E, particularly figures 1A and 5, (entire document) a light sensing element 1 formed in a semiconductor substrate 21; a sense node (gate of 2 in fig. 5) in electrical communication with said light sensing element for outputting a signal produced by said light sensing element; an amplification transistor 2 controlled by said

sense node, wherein said amplification transistor is a buried transistor 23 (MOS transistor in fig. 1A) formed in said semiconductor substrate.

With regards to claim 2, Inoue illustrates in fig. 5 and discloses in at least col. 5, lines 65-67, said light sensing element 1 is a photodiode.

With regards to claim 4, Inoue illustrates in fig. 5 said amplification transistor 2 outputs an amplified version of said signal to a column bit line 8.

With regards to claim 5, Inoue illustrates in fig. 5 a reset transistor 4 operative to reset said sense node to a reference voltage.

With regards to claim 6, the claimed "depletion mode transistor" is not considered to add any structure to the claimed device and is considered to be intended use of the device. It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. *Ex parte* Masham, 2 USPQ2d 1647 (1987).

Claims 7-12 are rejected under 35 USC § 102(b) as being anticipated by Matsunaga et al. ("Matsunaga") U.S. Patent No. 6,239,839.

With regards to claim 7, Matsunaga illustrates in figures 1-37, particularly figures 8, 34 and 35, (entire document) a light sensing element 62 formed in a semiconductor substrate 81; a sense node (gate of 64); a transfer transistor 306 operative to transfer a signal produced by said light sensing element to said sense node; and an amplification transistor 64 controlled by said sense node, wherein said amplification transistor is a body current transistor formed in said semiconductor substrate.

With regards to claim 8, Matsunaga illustrates in figs. 34 and 35, and discloses in at least col. 18, lines 35-54, said light sensing element 62 is a photodiode.

With regards to claims 9 and 12, Matsunaga discloses in at least the abstract said transfer transistor is a buried transistor (MOS-type).

With regards to claim 10, Matsunaga illustrates in figs. 34 and 35 said amplification transistor 64 outputs an amplified version of said signal to a column bit line 8.

With regards to claim 11, Matsunaga illustrates in figs. 34 and 35 a reset transistor 66 operative to reset said sense node to a reference voltage.

With regards to claim 12, the claimed "depletion mode transistor" is not considered to add any structure to the claimed device and is considered to be intended use of the device. It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. *Ex parte* Masham, 2 USPQ2d 1647 (1987).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 3 is rejected under 35 USC § 103 (a) as being unpatentable over Inoue as applied to claim 1 above, and further in view of Matsunaga. Inoue is discussed above, it does not show a transfer transistor. Matsunaga illustrates in figures 34 and 35 a transfer transistor 306. It would

have been obvious to one of ordinary skill in the art at the time the invention was made to have a transfer transistor to control charge from the light sensing element to the amplification transistor.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Hayashi and Ishida et al. (illustrate a photodiode and amplification transistor).

Field of Search	Date
U.S. Class and subclass: 257/428, 444, 461	November 8, 2004
Other Documentation: None	N/A
Electronic data base(s): EAST (USPAT, US-PGPUB, JPO, EPO, Derwent, IBM TDB)	November 8, 2004

Any inquiry concerning this communication or earlier communications from an examiner should be directed to Primary Examiner Allan Wilson whose telephone number is (571) 272-1738. Examiner Wilson can normally be reached 7:00-4:00 Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Allan R. Wilson
Primary Examiner
November 8, 2004